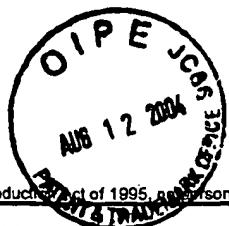


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Sheet 1

of 4

**Complete if Known**

Application Number	10/618,462
Filing Date	07/11/2003
First Named Inventor	Guangming Yin
Art Unit	2817
Examiner Name	Nguyen, Patricia T.
Attorney Docket Number	BP1817CON1

**U. S. PATENT DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> ( <i>if known</i> )			
PN		US- 5,345,449	09-06-1994	Inmos Limited	
PN		US- 5,420,529	05-30-1995	Northern Telecom Limited	
PN		US- 5,675,584	10-07-1997	Sun Microsystems, Inc.	
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PN		US- 6,222,380 B1	04-24-2001		
PN		US- 6,265,898 B1	07-24-2001		
PN		US- 6,463,092 B1	10-08-2002	Silicon Image, Inc.	
		US-			

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Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T <sup>6</sup>
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> ( <i>if known</i> )				

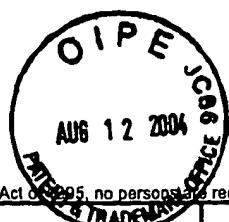
Examiner Signature	Patricia Nguyen	Date Considered	10/25/2004
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Application Number	10/618,462
Filing Date	07/11/2003
First Named Inventor	Guangming Yin
Art Unit	2816
Examiner Name	Nguyen, Patricia T.
Attorney Docket Number	BP1817CON1

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**NON PATENT LITERATURE DOCUMENTS**

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
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PN		MIZUNO, A GHzMOS Adaptive Pipeline Technique Using MOS Current-Mode Logic, IEEE Journal of Solid-State Circuits, vol. 31, No. 6, pp 784-791 (June 1996)	
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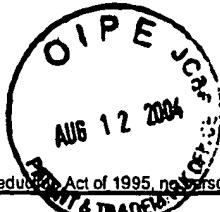
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Application Number	10/618,462
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Attorney Docket Number	BP1817CON1

**NON PATENT LITERATURE DOCUMENTS**

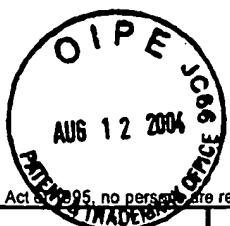
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PN		KURISU et al., 2.8Gb/s 176mW Byte-Interleaved and 3.0 Gb/s 118mW Bit-Interleaved 8:1 Multiplexers, 1996 International Solid state Circuits Conference pp. 122-23, 429	

Examiner Signature	<i>Patricia Nguyen</i>	Date Considered	<i>10/25/2004</i>
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Application Number

10/618,462

Filing Date

07/11/2003

First Named Inventor

Guangming Yin

Art Unit

2816

Examiner Name

Nguyen, Patricia T.

Attorney Docket Number

BP1817CON1

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PN		BAUMERT et al., A Monolithic 50-200 MHz CMOS Clock Recovery and Retiming Circuit, IEEE 1989 Custom Integrated Circuits Conference pp.14.5.1-14.5.4. (May 1989)	

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